## CLAIMS

What is claimed is:

1. An integrated circuit having multiple memory types comprising:

a first region having a plurality of transistors for implementing a non-volatile memory, the non-volatile memory comprising charge storing transistors, each of the charge storing transistors having three physically separate gate electrodes surrounding a channel and respective charge storage structures positioned around the channel and the three physically separate gate electrodes, a first gate electrode and a second gate electrode positioned adjacent opposite sidewalls of the channel and a third gate electrode overlying the channel, the third gate electrode receiving electrical bias to program and erase its respective underlying charge storage structure; and

a second region having a plurality of transistors for implementing a volatile memory, the volatile memory comprising charge storing transistors, each of the charge storing transistors having three physically separate gate electrodes surrounding a channel and respective charge storage structures positioned around the channel and the three physically separate gate electrodes, a first gate electrode and a second gate electrode positioned adjacent opposite sidewalls of the channel and a third gate electrode overlying the channel, each of the first and second gate electrodes receiving electrical bias to

program and erase a respective one of the underlying charge storage structures.

2 The integrated circuit of claim 1 wherein the channel for each of the plurality of transistors in the second region has a width that is different from channel widths for the plurality of transistors in the first region.

3. The integrated circuit of claim 1 wherein the channel for each of the plurality of transistors in the second region has a width that is less than channel widths for the plurality of transistors in the first region.

4. The integrated circuit of claim 1 further comprising:

a third region having a plurality of transistors, each of the plurality of transistors having three physically separate gate electrodes, wherein one, two or all of the three physically separate gate electrodes are biased.

5. The integrated circuit of claim 4 wherein all of the three physically separate gate electrodes are biased with a same valued voltage potential.

6. The integrated circuit of claim 4 wherein all of the three physically separate gate electrodes are biased with a different valued voltage potential.

7. An integrated circuit comprising:

a first memory including:

a first semiconductor structure including a top surface, a first sidewall, and a second sidewall opposing the first sidewall, the first semiconductor structure located in a first region of the integrated circuit;

a first charge storage structure located adjacent to the first sidewall;

a first gate structure located adjacent to the first charge storage structure on an opposite side of the first charge storage structure from the first sidewall;

a second memory including:

a second semiconductor structure including a top surface, a third sidewall, and a fourth sidewall opposing the third sidewall, the second semiconductor structure located in a second region of the integrated circuit;

a second charge storage structure located over the top surface of the second semiconductor structure;

a second gate structure located over the second charge storage structure, the first memory and the second memory being formed at different locations of a same substrate with a same process.

8. The integrated circuit of claim 7 wherein the second memory further comprises:

a third charge storage structure located adjacent to the third sidewall; and

a third gate structure located adjacent to the third charge storage structure on an opposite side of the third charge storage structure from the third sidewall.

9. The integrated circuit of claim 8 further comprising:

a first contact coupled to the first gate structure of the first memory, wherein no contact is coupled to the third gate structure of the second memory.

10. The integrated circuit of claim 7 wherein the first memory further comprises:

a third charge storage structure located over the top surface of the first semiconductor structure; and

a third gate structure located over the third charge storage structure.

11. The integrated circuit of claim 10 further comprising:

a first contact coupled to the second gate structure of the second memory, wherein no contact is coupled to the third gate structure of the first memory.

12. The integrated circuit of claim 7 wherein at least one of the first charge storage structure and the second charge storage structure includes nanoclusters.

13. The integrated circuit of claim 12 wherein the nanoclusters comprise at least one of silicon nanocrystals, germanium nanocrystals, silicon-germanium alloy nanocrystals, gold nanocrystals, silver nanocrystals, and platinum nanocrystals.

14. The integrated circuit of claim 7 further comprising:

a third charge storage structure located adjacent to the second sidewall; and

a third gate structure located adjacent to the third charge storage structure on an opposite side of the third charge storage structure from the second sidewall.

15. A method for implementing multiple memory types on an integrated circuit comprising:

providing a first region of the integrated circuit having a plurality of transistors for implementing a non-volatile memory, the non-volatile memory comprising a first plurality of charge storing transistors, each of the first plurality of charge storing transistors formed by the method of:

providing a substrate;

forming three physically separate gate electrodes overlying the substrate, the three physically separate gate electrodes surrounding a channel and at least one charge storage structure positioned around the channel and at least one

of the three physically separate gate electrodes, a first gate electrode and a second gate electrode positioned adjacent opposite sidewalls of the channel and a third gate electrode overlying the channel;

providing electrical contact to the third gate electrode for receiving electrical bias for programming and erasing;

providing a second region of the integrated circuit having a plurality of transistors for implementing a volatile memory, the volatile memory comprising a second plurality of charge storing transistors, each of the second plurality of charge storing transistors formed by the method of:

forming three physically separate gate electrodes overlying the substrate, the three physically separate gate electrodes surrounding a channel and at least one charge storage structure positioned around the channel and at least one of the three physically separate gate electrodes, a first gate electrode and a second gate electrode positioned adjacent opposite sidewalls of the channel and a third gate electrode overlying the channel; and

providing electrical contact to each of the first and second gate electrodes receiving electrical bias for programming and erasing.

16. The method of claim 15 further comprising:

forming a third region of the integrated circuit, the third region having a third plurality of transistors; and

forming the third plurality of transistors by forming each transistor with three physically separate gate electrodes surrounding a channel region by only a gate dielectric material.

17. The method of claim 16 further comprising:

biasing each of the three physically separate gate electrodes with a same bias voltage.

18. The method of claim 17 further comprising:

biasing only two of the three physically separate gate electrodes with a same bias voltage.

19. The method of claim 17 further comprising:

biasing each of the three physically separate gate electrodes with three different bias voltages.

20. The method of claim 15 further comprising:

forming each channel of the plurality of transistors in the first region with a width that is greater than each channel width of the plurality of transistors in the second region.